METHOD AND SYSTEM FOR DEVICE-LEVEL SIMULATION OF A CIRCUIT DESIGN FOR A PROGRAMMABLE LOGIC DEVICE

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ABSTRACT

A method and system for simulating a circuit design for a programmable logic device (PLD) at the device level. The same configuration data that is used to configure a PLD is used to generate objects that represent configurable logic elements of the PLD. During simulation, events are generated based on changes in output signal states of the objects. Each event includes an input signal state and identifies an object to which the input signal is to be applied. Since configurable logic elements are simulated, for example, lookup tables, instead of logic gates, fewer events need to be generated and processed than in a conventional simulator. In another embodiment, the system supports an interface that allows tools to interface with the simulator in the same manner as the tools interface with a PLD.